REMARKS/ARGUMENTS

Claims 1-25 are pending. Claims 1, 5, 7, 11, 13, 17 and 19 have been amended. New claims 20-25 have been added. Support for the amended and new claims is found in the specification. No new matter has been added.

Claims 1-19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Novak et al., (U.S. Patent Number 6,295,586). The applicants respectfully request reconsideration and allowance of the claims.

Claim Rejections - 35 U.S.C. § 102

Claim 1

The claims are allowable because each and every element is not shown or suggested by the prior art. For example, claim 1 recites, "an arbiter coupled to each of the plurality of memory transactions and configured to generate a plurality of bank readiness signals."

As described in the specification, the "present invention relates generally to interconnection architecture, and particularly to interconnecting multiple processors with multiple shared memories." (Specification at page 1, lines 2-3). In one embodiment, a queue includes a plurality of request stations 112A through 112N, each request station storing a memory transaction destined for one of a plurality of memory banks. As illustrated in figure 2, the arbiter is coupled to each of the plurality of memory transactions and generates bank readiness signals BNKRDYA through BNKRDYM. The arbiter selects one of the memory transactions from the queue based on the readiness of the memory banks to accept a memory transaction. (Specification at page 4, lines 19-30 and Figure 2). Because the arbiter is coupled to each of the plurality of memory transactions, the selection of a memory transaction is not limited the memory transaction stored in the final request station, for example, request station 712D in figure 7. (Specification at page 11, lines 13-25 and figure 7).

In contrast, Novak appears to discuss several queues (AQ, PQ, and RWQ) that are independently connected to the multiplexer SPM 370. (Novak at col. 8, line 66 to col. 9, line 5 and figure 2). "In the exemplary SMC 230, the AQ 340 and PQ 350 are each a one entry queue

and the RWQ 360 is a three entry queue." (Novak at col. 8, lines 3-5). As illustrated in figure 2 of Novak, only the bottom entry of each queue is connected to the multiplexer SPM. Taking the RWQ as an example, only the bottom entry of the RWQ is connected to the SPM. Thus, only a subset of the queue entries (the bottom entries) are connected to the SPM.

Therefore, in contrast with the present invention, Novak fails to teach or suggest "an arbiter coupled to each of the plurality of memory transactions and configured to generate a plurality of bank readiness signals," as recited by claim 1. For at least these reasons, claim 1 is in a condition for allowance.

Claims 2-6

Claims 2-6, which depend from claim 1, are in a condition for allowance, for at least the reasons discussed in relation to claim 1, as well as for the additional limitations they recite.

Claim 7

Claim 7 recites, "generating a plurality of bank readiness signals by monitoring the memory bus, each bank readiness signal indicating the readiness of one of the memory banks to accept a memory transaction." As illustrated in figure 2 of the present invention, in one embodiment, the state machine 204 "monitors the addresses of the memory transactions that are gated to memory 104" over memory bus 106. (Specification at page 5, lines 14-15).

Novak, on the other hand, discusses a memory controller in which the operation queues "assert a signal to the SPM" that "tells the SPM 370 that there is an operation ready to be sent." (Novak at col. 11, lines 11-15, emphasis added). Thus, "each operation queue is able to resolve timing and ordering dependencies and issue operations independently in order to initiate memory requests." (Novak at col. 11, lines 29-31, emphasis added). Nowhere does Novak teach or suggest "generating a plurality of bank readiness signals by monitoring the memory bus," as recited by claim 7. Because at least these claim elements are not taught or suggested by the prior art, claim 7 is in a condition for allowance.

Claims 8-12

Claims 8-12, which depend from claim 7, are in a condition for allowance, for at least the reasons discussed in relation to claim 7, as well as for the additional limitations they recite.

Claim 13

Claim 13 recites, "generating a plurality of bank readiness signals based upon a content of the memory bus." As discussed in relation to claim 7, Novak does not teach or suggest "generating a plurality of bank readiness signals based upon a content of the memory bus." For at least these reasons, claim 13 is in a condition for allowance.

Claims 14-18

Claims 14-18, which depend from claim 13, are in a condition for allowance, for at least the reasons discussed in relation to claim 13, as well as for the additional limitations they recite.

Claim 19

Claim 19 recites, "the product comprising instructions operable to ... generate a plurality of bank readiness signals based upon a content of the memory bus." As discussed in relation to claims 7 and 13, Novak does not teach or suggest at least these claim limitations. For at least these reasons, claim 19 is in a condition for allowance.

New Claims

Claims 20-25 have been added to more distinctly claim the present invention. The applicants respectfully submit that claims 20-25 are allowable because the recited claim elements are not shown or suggested by the prior art.

CONCLUSION

In view of the foregoing, applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400, extension 5518.

Respectfully submitted,

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